REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1, 2, 4-8, 10-20, and 22-30 are currently pending, with Claims 11-20 being withdrawn as directed to non-elected inventions. Claims 29 and 30 have been added; and Claims 1 and 22 have been amended by the present amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claim 1, 2, 7, 8, and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 3,866,029 to Chevalier et al. (hereinafter "the '029 patent") in view of the Tenemasa et al. reference ("Physical Random-Number Generator Using Schottky MOSFET"); Claims 4-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '029 patent in view of the Tenemasa et al. reference, further in view of U.S. Patent No. 5,222,142 to Kent (hereinafter "the '142 patent"); Claims 22 and 26-28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '029 patent in view of the Horowitz reference ("The Art of Electronics"); and Claims 23-25 were rejected under 35 U.S.C. §103(a) as being unpatentable over the '029 patent and the Horowitz reference, further in view of the '142 patent.

Amended Claim 1 is directed to a random number generator, comprising: (1) a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a count value of the clock signal with respect to a transition of the random signal; and (2) a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal, wherein the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which said random signal is supplied, and wherein when a frequency of the clock signal increases, a bias of a

frequency of occurrence of "0" and "1" becomes smaller. The changes to Claim 1 are supported by the originally filed specification and do not add new matter.[1]

Applicants respectfully submit that the rejection of Claim 1 (and all similarly rejected dependent claims) is rendered moot by the present amendment to Claim 1.

Regarding the rejection of Claim 1 under 35 U.S.C. §103(a), the Office Action asserts that the '029 patent discloses everything in Claim 1 with the exception of the counter circuit being a one bit counter, the count value of which alternates between a high level and a low level every one count, the counter circuit having a clock enable input through which the random signal is supplied, and relies on the Tenemasa et al. reference to remedy those deficiencies.

The '029 patent is directed to a random number generator for generating a sequence of binary random numbers whose expected value is controlled by an input digital number. As shown in the only figure in the '029 patent, the '029 patent discloses a binary counter 20, a latch 21, and a random bits generator 11. In particular, the '029 patent discloses that the binary counter 20 has four inputs: a clear input 14, a count input 16, a clock input, and an enable input 17. Further, as shown in the figure, the '029 patent discloses that the output 12 of the random bits generator 11 is input to the clear input of the binary counter, while the count input of the binary counter receives the inversion of the random signal 12, via the inverter 22.

In particular, the '029 patent discloses a four-bit counter 20 that requires a counter clear signal for operation. When the signal given to the enabling input 17 from the NB_i signal 13 is one and the signal given to the clear input 14 is one, the output C_i will be reset to zero. On the other hand, if the signal given to the count input 16 is one, the C_i output 25 will be reset to a clock pulse number that is fed to the clock input of the binary counter 20 from the

[1] See, e.g., page 10, lines 3-9 of the specification.

clock. In other words, the binary counter 20 counts the clock pulse number when the RB_i output 12 is in the zero state. Thus, if the binary counter is not reset by the counter clear signal, the range of errors will be up to 16 bits. Further, Applicants note that in binary counter 20 disclosed by the '029 patent, misalignment of the input timing may occur such that the state of the clear and count inputs is either 00 or 11. Thus, if another clock signal is fed to the binary counter 20 when the binary counter 20 is in one of these states, the binary counter 20 cannot override the counter value even if a new random signal is fed to the binary counter. Thus, the binary counter can't produce the appropriate random number. Applicants note that this misalignment is caused by having two inputs to the binary counter.

However, as admitted in the outstanding Office Action, the '029 patent fails to disclose that the counter circuit is a one-bit counter, the count value of which alternates between a high level and a low value every one count, the counter circuit having a clock enable input through which the random signal is supplied, as recited in amended Claim 1.

Further, Applicants respectfully submit that the '029 patent fails to disclose that when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller, as recited in amended Claim 1. Applicants respectfully submit that the '029 patent is silent regarding the relationship between the bias of the frequency of occurrence and the frequency of the clock signal, as that relationship is recited in amended Claim 1.

The Tenemasa et al. reference is directed to a physical random number generator using a reversely operated Schottky MOSFET. As shown in Figure 4, the random number generator includes a Schmidt triggered inverter and a JK flip-flop.

However, Applicants respectfully submit that the Tenemasa et al. reference fails to disclose that when a frequency of a clock signal increases, a bias of a frequency of the

occurrence of "0" and "1" becomes smaller, as required by amended Claim 1. Applicants respectfully submit that the Tenemasa et al. reference is silent regarding this limitation.

Thus, no matter how the teachings of the '029 patent and the Tenemasa et al. reference are combined, the combination does not teach or suggest a random number generator in which when a frequency of the clock signal increases, a bias of the frequency of occurrence of "0" and "1" becomes smaller, as recited in amended Claim 1. Accordingly, Applicants respectfully submit that amended Claim 1 (and all similarly rejected dependent claims) patentably defines over any proper combination of the '029 patent and the Tenemasa et al. reference.

Independent Claim 22 is directed to a random number generator comprising: (1) a counter circuit configured to be supplied with a clock signal and a random signal, and to provide a counter value of the clock signal with respect to a transition of the random signal; (2) a first latch circuit configured to latch the count value with respect to the transition of the random signal, and to output a first random number signal; and (3) a source for the random signal adapted to produce said random signal having a characteristic in which power spectrum intensity decreases with increasing frequency, wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal, and wherein when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller.

As discussed above, the '029 patent is directed to a random number generator for generating a sequence of binary random numbers whose expected value is controlled by an input digital number.

However, as admitted in the outstanding Office Action, the '029 patent fails to disclose that a source for the random signal is attached to produce the random signals having

a characteristic in which the power spectrum intensity decreases with increasing frequency, wherein the source comprises an oscillation circuit using a delay time of a CR delay circuit, and wherein random variations of the resistance and capacitor values of the CR delay circuit are used for generating the random signal.

Further, Applicants respectfully submit that the '029 patent fails to disclose that when a frequency of the clock signal increases, a bias of the frequency of occurrence of "0" and "1" becomes smaller, as recited in amended Claim 22.

Applicants respectfully submit that the Horowitz reference fails to remedy the deficiencies of the '029 patent with respect to this limitation. In particular, Applicants respectfully submit that the Horowitz reference is silent regarding when a frequency of a clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller, as recited in amended Claim 22.

Thus, no matter how the teachings of the '029 patent and the Horowitz reference are combined, the combination does not teach or suggest that when a frequency of the clock signal increases, a bias of a frequency of occurrence of "0" and "1" becomes smaller, as recited in amended Claim 22. Accordingly, Applicants respectfully submit that amended Claim 22 (and all similarly rejected dependent claims) patentably defines over any proper combination of the '029 patent and the Horowitz reference.

Regarding the rejection of dependent Claims 4-6 and 23-25 under 35 U.S.C. §103(a), Applicants respectfully submit that the '142 patent fails to remedy the deficiencies of the '029 patent, the Tenemasa et al. reference, and the Horowitz reference, as discussed above. Accordingly, Applicants respectfully submit that the rejections of dependent Claims 4-6 and 23-25 are rendered moot by the present amendment to independent Claims 1 and 22.

The present amendment also sets forth new Claims 29 and 30 for examination on the merits. New Claims 29 and 30 are supported by the originally filed specification and do not add new matter.[2]

Thus, it is respectfully submitted that independent Claims 1, 22, 29, and 30 (and all associated dependent claims) patentably define over any proper combination of the cited references.

Consequently, in view of the present amendment and in light of the above discussion, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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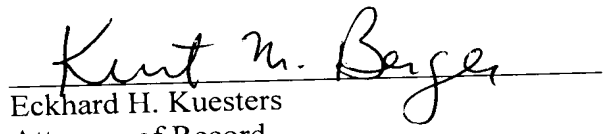

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[2] See page 11, lines 14-17 of the specification.